

HALL TICKET NUMBER

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PACE INSTITUTE OF TECHNOLOGY & SCIENCES::ONGOLE
(AUTONOMOUS)

II B.TECH I SEMESTER END SUPPLEMENTARY EXAMINATIONS, JAN - 2023
SWITCHING THEORY AND LOGIC DESIGN
(ECE Branch)

Time: 3 hours

Max. Marks: 60

Note: Question Paper consists of Two parts (Part-A and Part-B)

PART-A

Answer all the questions in Part-A (5X2=10M)

Q.No.	Questions	Marks	CO	KL
1	a) Compute the subtraction for 11011 – 10100 using 2's complement.	[2M]	1	
	b) Simplify the Boolean function $F(x, y, z) = \sum(3, 4, 6, 7)$ using K-map,	[2M]	2	
	c) Write differences between the decoder and multiplexer.	[2M]	3	
	d) Define flip-flop and list the various types of flip-flops.	[2M]	4	
	e) Draw the four-bit shift register.	[2M]	5	

PART-B

Answer One Question from each UNIT (5X10=50M)

Q.No.	Questions	Marks	CO	KL
UNIT-I				
2.	a) Express the following numbers in decimal: (i) $(10010.0100)_2$ (ii) $(36.12)_8$.	[5M]	1	
	b) Implement the Boolean function: $F = xy + x'y' + y'z$ using with NAND and inverter gates.	[5M]	1	
OR				
3.	a) Find the 1's and 2's complements of the following binary numbers: (i) 11000101 (ii) 10100000	[5M]	1	
	b) Express the complement of the following functions in sum-of-minterms form: $F(A, B, C, D) = \sum(2,4,7,10,12,14)$	[5M]	1	
UNIT-II				
4.	a) Simplify the following Boolean function using <i>Karnaugh</i> maps: $F(w, x, y, z) = \sum(1, 4, 5, 6, 12, 14, 15)$	[5M]	2	
	b) Draw and explain the implementation of full adder with two half adders and an OR gate.	[5M]	2	
OR				
5.	a) Simplify the following Boolean functions using <i>Karnaugh</i> maps: $F = A'B'C' + B'CD' + A'BCD' + AB'C$	[5M]	2	
	b) Draw and explain the carry lookahead generator.	[5M]	2	
UNIT-III				
6.	a) Define decoder. Construct 3x8 decoder using logic gates.	[5M]	3	
	b) With neat sketches explain the Programmable Logic Array (PLA).	[5M]	3	
OR				
7.	a) Explain the 4 x 16 decoder constructed with two 3 x 8 decoders.	[5M]	3	
	b) Implement the following two Boolean function with a PLA: $F_1(A, B, C) = \sum(0, 1, 2, 4)$	[5M]	3	
UNIT-IV				
8.	a) Discuss about basic architectural distinctions between combinational and sequential circuits.	[5M]	4	

	b)	Draw and explain the clocked J-K Flip-Flop with truth table.	[5M]	4	
OR					
9.	a)	Draw and explain the D -type positive-edge-triggered flip-flop.	[5M]	4	
	b)	Explain the Master-slave JK flip-flop with neat diagrams.	[5M]	4	
UNIT-V					
10.	a)	Explain about Ring and Johnson Counter using Shift Register	[5M]	5	
	b)	Explain the following related to sequential circuits with suitable examples. (i) State diagram. (ii) State table.	[5M]	5	
OR					
11.	a)	Design a four-bit binary synchronous counter with <i>D</i> flip-flops.	[5M]	5	
	b)	What are the capabilities and limitations of finite state machines? Discuss.	[5M]	5	
